CLAIMS

What is claimed is:

1. A method of generating synthesis scripts to synthesize integrated circuit (IC) designs from a generic netlist description into gate-level description, said method comprising the steps of:

identifying hardware elements in the generic netlist;

determining key pins for each of said identified hardware elements;

extracting design structure and hierarchy from the Generic netlist;

generating script to cause a logic synthesis tool to apply bottom-up synthesis to modules and sub-modules of the IC design;

generating script to cause a logic synthesis tool to apply top-down characterization to modules and sub-modules of the IC design; and

generating script to cause a logic synthesis tool to repeat said bottom-up and said top-down applications until constraints are satisfied.

2. A method according to claim 1 wherein said step of extracting design structure allows for a multilevel structuring of modules of the IC design.

3. A method according to claim 1 further comprising the step of generating script to cause a logic synthesis tool to apply initial mapping to the IC design.

4. A method according to claim 1 wherein the logic synthesis tool is Synopsys Design Compiler.

5. A method according to claim 1 further comprising the step of rearranging design hierarchy by changing the design.

6. A method according to claim 1 further comprising the step of generating

script to cause a logic synthesis tool to ungroup modules of the IC design.

7. A synthesis script generation tool, comprising:

extractor to extract synthesis-related design information from a file having the design information;

target technology library to provide technology cells and hardware characteristics of the cells for the purposes of mapping the design to the technology; and

script generator for a logic synthesis tool.

8. A tool according to claim 6 wherein the logic synthesis tool is Synopsys Design Compiler.

9. An apparatus for generating synthesis scripts to synthesize integrated circuit (IC) designs in RTL level description into gate-level description, comprising:

a processor;

memory connected to said processor;

said memory having instructions for said processor to

determine key pins for each of said identified hardware elements;

extract critical design structure and hierarchy from the generic netlist;

apply bottom-up synthesis to modules and sub-modules of the IC design;

apply top-down characterization to modules and sub-modules of the IC design;

repeat said bottom-up and said top-down applications until constraints are satisfied; and

create design compile scripts to synthesize modules and sub-modules and the IC design having said satisfied constraints.

10. An apparatus for generating synthesis scripts to synthesize integrated circuit (IC) designs in RTL level description into gate-level description, comprising:

means for determining key pins for each of said identified hardware elements;

means for extracting critical design structure and hierarchy from the generic netlist;

means for applying bottom-up synthesis to modules and sub-modules of the IC design;

means for applying top-down characterization to modules and sub-modules of the IC design;

means for repeating said bottom-up and said top-down applications until constraints are satisfied; and

means for creating design compile scripts to synthesize modules and sub-modules and the IC design having said satisfied constraints.

11. A computer storage medium containing instructions for generating synthesis scripts to synthesize integrated circuit (IC) designs in RTL level description into gate-level description, said instructions comprising the steps of:

identifying hardware elements in the generic netlist;

determining key pins for each of said identified hardware elements;

extracting critical design structure and hierarchy from the generic netlist;

applying bottom-up synthesis to modules and sub-modules of the IC design;

applying top-down characterization to modules and sub-modules of the IC design;

repeating said bottom-up and said top-down applications until constraints are satisfied; and

creating design compile scripts to synthesize modules and sub-modules and the IC design having said satisfied constraints.

12. A computer storage medium of claim 11 wherein said computer storage medium is selected from a group consisting of magnetic device, optical device, magneto-optical device, floppy diskette, CD-ROM, magnetic tape, computer hard drive, and memory card.

13. A process for generating synthesis scripts to synthesize integrated circuit (IC) designs in RTL level description into gate-level description, said process comprising the steps of:

identifying hardware elements in the generic netlist;

determining key pins for each of said identified hardware elements;

extracting critical design structure and hierarchy from the generic netlist;

applying bottom-up synthesis to modules and sub-modules of the IC design;

applying top-down characterization to modules and sub-modules of the IC design;

repeating said bottom-up and said top-down applications until constraints are satisfied; and

creating design compile scripts to synthesize modules and sub-modules and the IC design having said satisfied constraints.

14. A computer system for generating synthesis scripts to synthesize integrated circuit (IC) designs in RTL level description into gate-level description, said system comprising:

means for determining key pins for each of said identified hardware elements;

means for extracting critical design structure and hierarchy from the generic netlist;

means for applying bottom-up synthesis to modules and sub-modules of the IC design;

means for applying top-down characterization to modules and sub-modules of the IC design;

means for repeating said bottom-up and said top-down applications until constraints are satisfied; and

means for creating design compile scripts to synthesize modules and sub-modules and the IC design having said satisfied constraints.